7. ELECTRICAL CHARACTERISTICS

(T_{amb} = −20 to 60℃)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
System	Analog/ Logic Vol.	VDD_3.3V	-	3.0	3.3	3.6	VDC	
Panel	Analog/ Logic Vol	ELVDD			4.6			
	Analog/ Logic Vol	ELVSS			(-2.3)			
Battery	Analog Vol.	VBAT	-	5.5	-	21	VDC	(4)
Input Voltage	H-level	VIH	-	0.7xVDD_1.8	-	VDD_1.8	VDC	
	L-level	VIL	-	Vss	-	0.3xVDD_1.8	VDC	
Output Voltage	H-level	VOH	IOH = -2/4/8/12mA	0.8xVDD_1.8	-	VDD_1.8	VDC	
	L-level	VOL	IOH = -2/4/8/12mA	Vss	-	0.2xVDD_1.8	VDC	
Current	Logic	IVDD_3.3V	Full White VDD_3.3V=3.3V VBAT=10V	(541)	(636)	(697)	mA	(1) (2) (3)
	Panel	IVBAT		(425)	(500)	(560)		
Consumption	Logic	PVDD_3.3V		(1.78)	(2.1)	(2.3)	W	(1) (3)
	Panel	PVBAT		(4.25)	(5.0)	(5.6)		
Frame Frequency		fFRM	-	-	120	-	Hz	

Only for HP

Note(1) : VDD_3.3V=3.3(V), Full White pattern. Temperature = 22±3℃ Room Temperature

Note(2) : Measured using SDC Standard Operating Circuit
Current Consumption could be different under customer's DC-DC circuit design.

Note(3) : This data is a calculated value. SDC is managed based on Vbat=10V.

Note(4) : For 5.5V to 6.0V VBAT, current should be 650mA(TBD).

"The Fuse is not intended to be replaced."

9. INPUT TERMINAL PIN ASSIGNMENT

. INPUT SIGNAL (eDP, Connector : HIROSE KN38A-40S-0.5H Locking type)

Pin No.	Signal name	Description
1	ELVSS	Power for Panel
2	ELVSS	Power for Panel
3	NC	NC
4	ELVDD	Power for Panel
5	ELVDD	Power for Panel
6	NC (HSYNC)	Touch vendor can use to avoid noise. Do not use for other purpose(1.8V).
7	EL_ON2	Enable for EL PMIC(1.8V)
8	LOGIC_GND	Logic and driver ground
9	LOGIC_GND	Logic and driver ground
10	LOGIC_GND	Logic and driver ground
11	NC	Do not used. Test pin for display.
12	NC	Do not used. Test pin for display.
13	NC	Do not used. Test pin for display.
14	NC	Do not used. Test pin for display.
15	NC	Do not used. Test pin for display.
16	NC	Do not used. Test pin for display.
17	NC	Do not used. Test pin for display.
18	H_GND	eDP signal ground
19	DP_3N	eDP negative signal Lane3
20	DP_3P	eDP positive signal Lane3
21	H_GND	eDP signal ground
22	DP_2N	eDP negative signal Lane2
23	DP_2P	eDP positive signal Lane2
24	H_GND	eDP signal ground
25	DP_1N	eDP negative signal Lane1
26	DP_1P	eDP positive signal Lane1
27	H_GND	eDP signal ground
28	DP_0N	eDP negative signal Lane0
29	DP_0P	eDP positive signal Lane0
30	H_GND	eDP signal ground
31	AUX_P	eDP AUX positive signal
32	AUX_N	eDP AUX negative signal
33	H_GND	eDP signal ground
34	NC	-
35	VCC_3.3V	Logic and driver power
36	VCC_3.3V	Logic and driver power
37	VCC_3.3V	Logic and driver power
38	BIST_EN	BIST enable signal(1.8V)
39	HPD	HPD signal(3.3V)
40	EL_ON3	EL Enable signal(1.8V)

Only for HP

10-3 POWER ON/OFF SEQUENCE

10-3.1 Power On Sequence

	Sequence	
1	Power Off Status	
2	System Power on (Turn on VBAT and Turn on VCC_3.3V simultaneously)	Note1, 2
3	Wait HPD (L → H)	Note1, 2
4	Link Training	Note1, 2
5	Brightness Control	Note 2
6	ELP Control	
7	Data Stream	Note1, 2
8	Display On (EL_ON3 = H)	Note1, 2
9	Display On Status	

10-3.2 Power Off Sequence

	Sequence	
1	Power on Status	
2	Display Off (EL_ON3 = L)	Note1, 3
3	Wait 150ms	Note1, 3
4	System Power Off (Turn off VBAT and Turn off VCC_3.3V simultaneously)	Note1, 3
5	Power Off Status	

Only for HP

Appendix - Operating Code

ATNA40CU03

(eDP)

Operating Code

Rev.A

Only for HP

- **Table of Contents**

1. Model Information 37
2. Revision History 37
3. Operating Sequence 38
3.1 Power On Sequence 38
3.2 Power Off Sequence 38
4. Brightness Control 41
4.1 Brightness Control for Intel 41
4.2 Brightness Control for nVidia 41
4.3 Brightness Control for AMD 41
5. ELP (Edge Luminance Profile) Control 42

1. Model Information

Model	ATNA40CU03 (PID 4197)	
T-con	ANA38407 (ANAPASS)	
EL PMIC	SM3201C (Silicon Mitus)	
Resolution	2880(H) x 1800(V)	
Condition	**GPU**	Intel ADL (Window OS) nVidia AMD RBR (Window OS)
	I/F	eDP 4Lane
	eDP Speed	8.1 Gbps
	Frame Freq.	48~120Hz VRR
	Porch (Video only)	H blank 100
		V blank 24
Input Voltage	**VBAT**	6.0V~21.0V
	VCC_3.3V	Typ. 3.3V

2. Revision History

Rev.	Date	Description	Checked by
Rev. A	22.06.15	- Initial Release	HG Kim

Only for HP

3. Operating Sequence

3.1 Power On Sequence

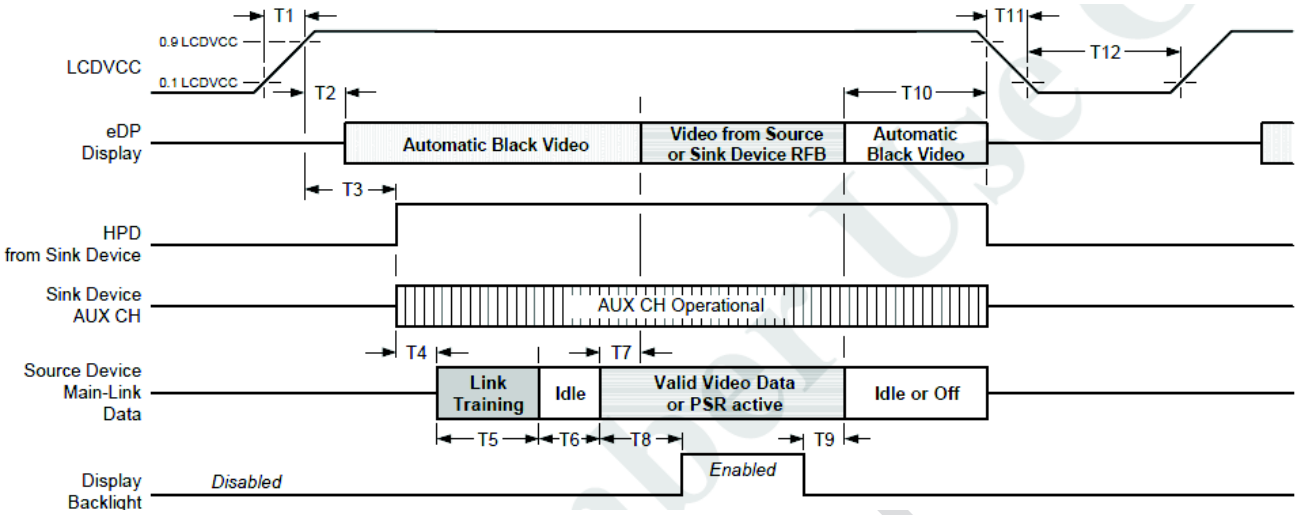
	Sequence	
1	Power Off Status	
2	System Power on (Turn on VBAT and Turn on VCC_3.3V simultaneously)	Note1,2
3	Wait HPD (L → H)	Note1,2
4	Link Training	Note1,2
5	Brightness Control	Note2
6	ELP Control	
7	Data Stream	Note1,2
8	Display On (EL_ON3 = H)	Note1,2
9	Display On Status	

3.2 Power Off Sequence

	Sequence	
1	Display On Status	
2	Display Off (EL_ON3 = L)	Note1,3
3	Wait 150ms	Note1,3
4	System Power Off (Turn off VBAT and Turn off VCC_3.3V simultaneously)	Note1,3
5	Power Off Status	

Only for HP

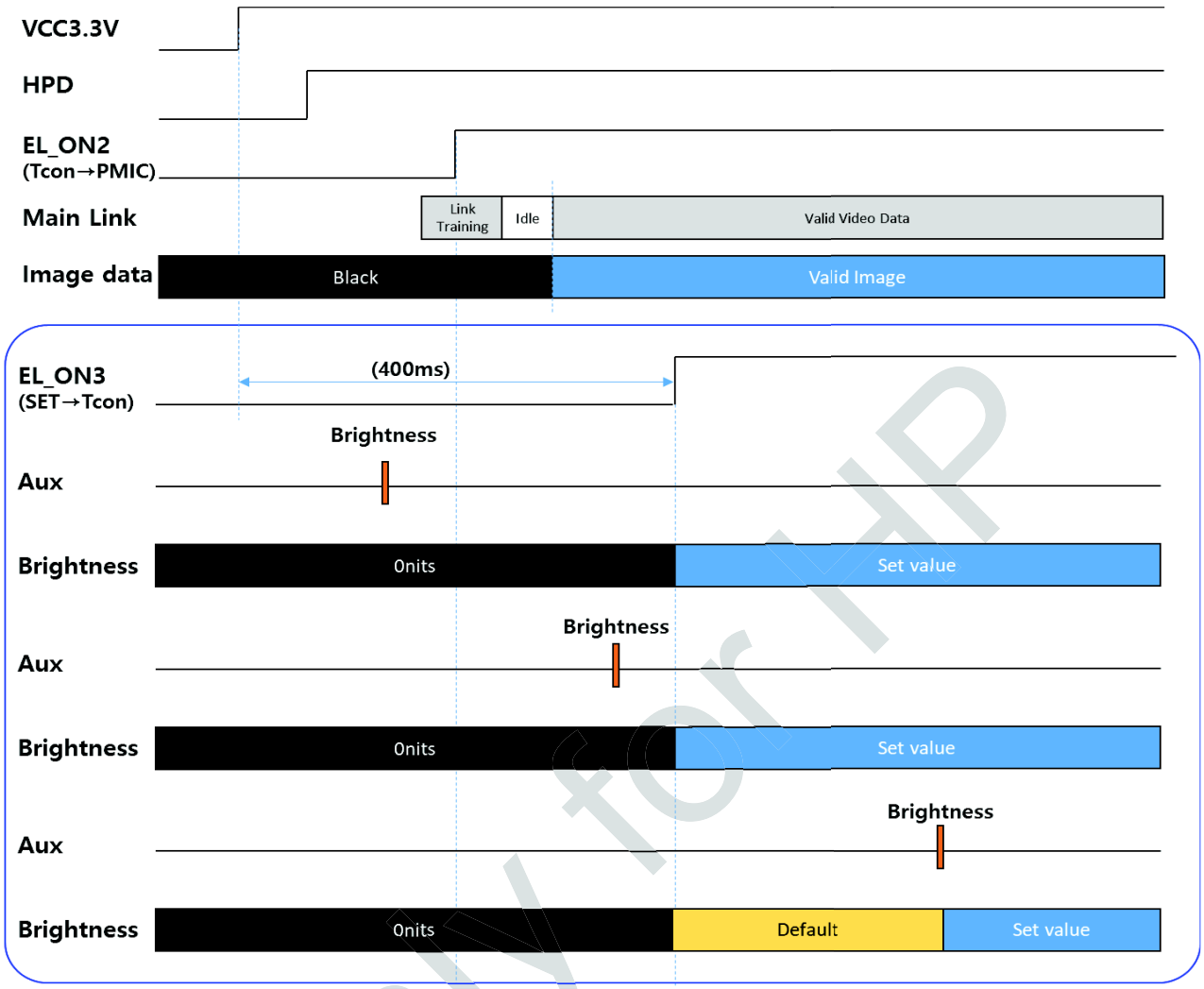
Note1) Power on/off Timing



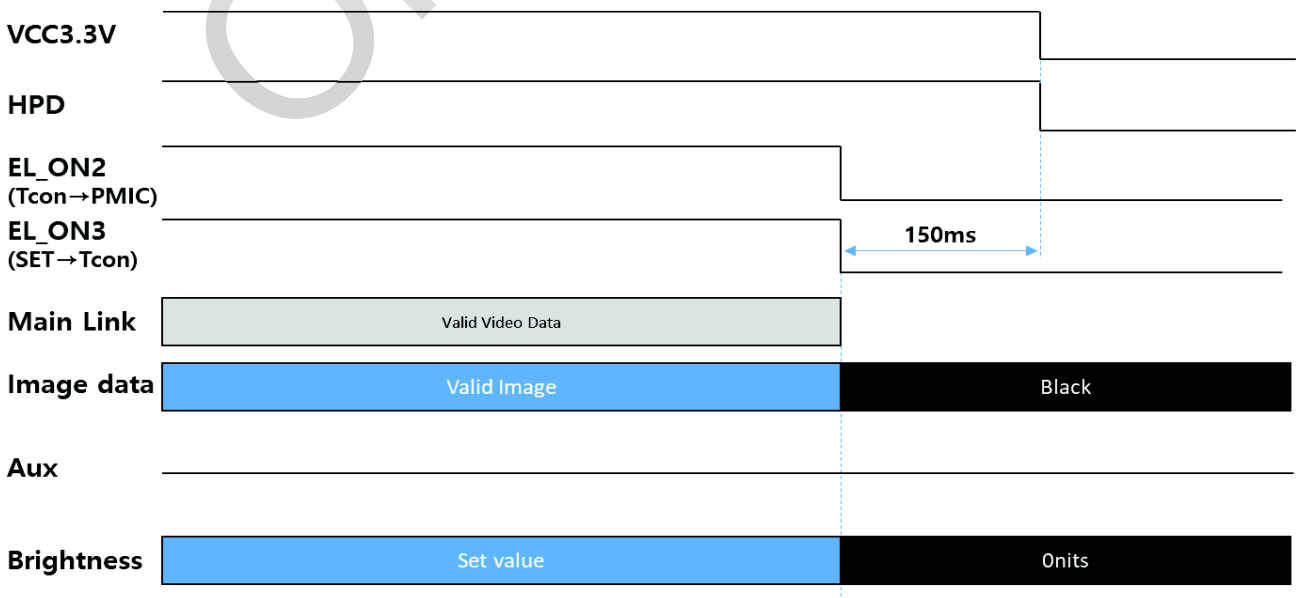
Timing Para.	Description	Min (ms)	Max (ms)	Notes
T1	Power rail rise time, 10% to 90%	0.5	10	
T2	VCC ~ Automatic Black Video	0	80	
T3	VCC ~ HPD high	0	80	
T4	HPD high ~ Link Training initialization	-	-	
T5	Link Training	-	-	
T6	Link idle	-	-	
T7	Valid Video Delay (or PSR active) from source to display	0	50	
T8	Valid Video ~ Display On	-	-	EL_ON3 = H Refer to Note2 in detail
T9	Display Off ~ Automatic Black Video	-	-	EL_ON3 = L Refer to Note3 in detail
T10	Automatic Black Video ~ Power Off	150	500	
T11	Power rail fall time, 90% to 10%	-	10	
T12	Power Off Time	500	-	

Only for Customer Use

Note2) Example of power on sequence in detail



Note3) Example of power off sequence in detail



Only for HP

4. Brightness Control

4.1 Brightness Control for Intel

Addr.	R/W	Values	Description
0x0354 0x0355	R/W	{ 0xXX, 0xXX }; /* 0x90, 0x01 : 400nit */ /* 0x96, 0x00 : 150nit */ /* 0x04, 0x00 : 4nit */	DPCD_INTEL_EDP_BRIGHTNESS_NITS {LSB, MSB} of nits value
0x0356		{ 0xXX }; /*0x00 : immediately */	Number of frames over which the change should be applied
0x0357		{ 0xXX }; /*0x00 : immediately */	Per frame steps to be applied Write to 357h is the trigger for TCON to consider the new nits value

4.2 Brightness Control for nVidia

Addr.	R/W	Values	Description
0x0721	W	{ 0x02 }	EDP_BACKLIGHT_MODE_SET Write to 721h is the trigger for TCON to consider the new nits value
0x0722 0x0723	W	{ 0xXX, 0xXX }; /* 0x07, 0xFF : 100% (400nit) */ /* 0x02, 0xFF : 37.5% (150nit) */ /* 0x00, 0x14 : 1.0% (4nit) */	EDP_BACKLIGHT_BRIGHTNESS {MSB, LSB} of percentage value Write to 723h is the trigger for TCON to consider the new nits value

4.3 Brightness Control for AMD

Addr.	R/W	Values	Description
0x0320 0x0321 0x0322 0x0323	W	{ 0xXX, 0xXX, 0xXX, 0xXX }; /* 0x80, 0x1A, 0x06, 0x00 : 400nit */ /* 0xF0, 0x49, 0x02, 0x00 : 150nit */ /* 0xA0, 0x0F, 0x00, 0x00 : 4nit */	32bit requested brightness in millinits – Byte0(LSB) ~ Byte3(MSB)

[Table 1. Recommended Nit Range]

Nit Range	Step Size (nit)
[4, 100]	1
[100, 300]	5
[300, 400]	10

Only for HP

5. ELP (Edge Luminance Profile) Control

4.1 Brightness Control for Intel

Addr.	R/W	Values	Description
0x402E	W	{ 0xXX } /* 0x00 : ELP off * /* 0xC0 : ELP 20% on */	ELP off / on

Only for HP